

CLAIMS

What is claimed is:

[0098] 1. A hierarchical test control network for an integrated circuit,
5 comprising:

 a top-level test control circuit block, said top-level test control circuit block
comprising a chip access port (CAP) controller; and

 a plurality of lower-level test control circuit blocks connected to said top-level
test control circuit block in a hierarchical structure, each of said lower-level test
10 control circuit blocks comprising a socket access port (SAP) controller;

 wherein test operation is transferred downward and upwards within said
hierarchical structure.

[0099] 2. A hierarchical test control network for a chip design, comprising:

15 a plurality of test control circuit blocks in a hierarchical structure having a
plurality of hierarchical levels, said test control circuit blocks comprising
 a top-level test control circuit block having a chip access port (CAP)
controller; and

20 a plurality of lower-level test control circuit blocks, one or more of said
lower-level test control circuit blocks at each of said hierarchical levels, at
least one of said lower-level test control circuit blocks connected to said top-
level test control circuit block, each of said lower-level test control circuit
blocks comprising a socket access port (SAP) controller;

wherein test operation is transferred downward and upwards within said hierarchical structure by communicating from each test control circuit block to the test control circuit block at the immediately higher or immediately lower hierarchical level in said hierarchical structure.

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[0100] 3. The hierarchical test control network of claim 2 wherein said hierarchical structure is organized in a plurality of tiers, and wherein the lower-level test control circuit blocks are connected in a serial chain, one of said lower-level test control circuit blocks at each tier of the hierarchical structure.

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[0101] 4. The hierarchical test control network of claim 2 wherein said hierarchical structure is organized in a plurality of tiers, and wherein the lower-level test control circuit blocks are connected in a serial chain, one or more of said lower-level test control circuit blocks are connected at any given tier of said hierarchical network.

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[0102] 5. The hierarchical test control network of claim 2, wherein each of said lower-level test control circuit blocks is connected to a different virtual circuit block for controlling testing thereof.

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[0103] 6. The hierarchical test control network of claim 2, wherein each of said lower-level test control circuit blocks comprises a test mode select input port, a test data input port, and a test data output port.

[0104] 7. The hierarchical test control network of claim 6, wherein each of said lower-level test control circuit blocks comprises a test access port state controller for controlling the receipt or transmission of information from or to the test mode select input port, the test data input port, and the test data output port.

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[0105] 8. The hierarchical test control network of claim 2, wherein all of the lower-level test control circuit blocks connected at the same hierarchical level share a common test mode enable input signal, a common test reset signal, a common test mode select signal, and a common clock signal.

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[0106] 9. The hierarchical test control network of claim 8, wherein all of the lower-level test control circuit blocks connected at the same hierarchical level collectively output a common test mode data output signal comprising a logical OR of individual test mode data output signals output from each of the lower-level test control circuit blocks connected at the same hierarchical level.

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[0107] 10. The hierarchical test control network of claim 9, wherein each of the lower-level test control circuit blocks connected at the same hierarchical level receives separate test mode data input signals from lower-level test control circuit 20 blocks at an immediately lower hierarchical level, and outputs separate test mode enable output signals to the lower-level test control circuit blocks at the immediately lower hierarchical level.

[0108] 11. The hierarchical test control network of claim 2, wherein all of the lower-level test control circuit blocks of the hierarchical test control network are functionally identical.

5 **[0109]** 12. The hierarchical test control network of claim 2, wherein all of the lower-level test control circuit blocks are structurally identical.

[0110] 13. A hierarchical test control network for an integrated circuit, comprising:

10 a plurality of test control circuit blocks arranged in a hierarchical structure having a plurality of hierarchical levels, each of said test control circuit blocks comprising a first test data input port, a second test data input port, and a test data output port, at least one of said test control circuit blocks connected to a chip access port;

15 a common test mode select signal connected to all of said test control circuit blocks;

a common test reset signal connected to all of said test control circuit blocks; and

a common test clock signal connected to all of said test control circuit blocks;

20 wherein test control circuit blocks at the same hierarchical level each receive at their second test data input port a shared test data output signal from the test data output port of a test control circuit block at the immediately higher hierarchical level,

said test control circuit blocks at said same hierarchical level connected in a chain configuration.

[0111] 14. The hierarchical test control network of claim 13, wherein said test control circuit blocks comprise:

5 a top-level test control circuit block having a chip access port (CAP) controller connected to said chip access port; and

a plurality of lower-level test control circuit blocks, one or more of said lower-level test control circuit blocks at each of said hierarchical levels, at least one of said lower-level test control circuit blocks connected to said top-level test control circuit 10 block, each of said lower-level test control circuit blocks comprising a socket access port (SAP) controller;

wherein test operation is transferred downward and upwards within said hierarchical structure by communicating from each test control circuit block to the test control circuit block at the immediately higher or immediately lower hierarchical level

15 in said hierarchical structure.